Remarks

Claims 1, 3, 4, 6-8, and 10-20 are pending in this application. Claim 5 has been cancelled herein. Claims 1, 6, 7, and 17 have been amended. The Examiner has rejected claims 1 and 4-6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Publication No. 2003/0046464 to Murty et al. (hereinafter "Murty"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. (hereinafter "Carmean"). Further, claims 7-15, 17, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of U.S. Patent No. 6,857,084 to Giles (hereinafter "Giles"). Finally, claims 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of Giles and further in view of Carmean.

A. Claims rejected under 35 U.S.C. 102

Claims 1, 4, 5, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Murty. Because the Examiner rejected independent claim 1 under section 102(b) on the basis of Murty, each element of the claim must be disclosed in Murty. Murty, however, does not disclose each element of independent claim 1, as amended.

First, Murty does not disclose the claimed element of the non-interrupt-handling processors being operable to be serially released from the interrupt mode according to a **timed release basis**. In accordance with the present invention, the non-interrupt-handling processors exit from the interrupt mode on a serial basis according to a **time delay managed** by the interrupt handling processor. (Summary, page 4, lines 16-18). Additionally, independent claim 1 is currently amended to recite that the interrupt-handling processor (the "assigned processor" in this claim) is operable to initiate the release of **every other** processor (the non-interrupt-handling processors) from the interrupt mode on a **timed release basis**. In the Response to Arguments

section, the Examiner states that the time delayed serial release of the **non-interrupt-handling** processors is not recited in the rejected claims. Claim 1 has been amended such that this element is now recited, as stated above.

Murty fails to teach or disclose releasing non-interrupt handling processors serially from the interrupt handling mode according to a **timed release basis.** The Examiner points to paragraph [0046] of Murty as teaching this limitation. However, this paragraph states only that the mechanisms for resetting the single flag of Murty "assume that the time between common interrupts is typically greater than the time necessary for all of the logical processors to execute the interrupt handler (or portions thereof) and access the flag." (Murty, [0046]) As stated in the Amendment and Remarks of the previously filed Request for Continued Examination, the time discussed in this passage is the time **between interrupts**, and **not** the **time delay** between releasing non-interrupt handling processors. When Murty does mention the time necessary for the processors to execute the interrupt handler, it is only with reference to an **aggregate** amount of time required for **all** of the processors to perform a task, and this in no way teaches or discloses a **timed release basis** for releasing non-interrupt processors serially from the interrupt handling mode. The Examiner failed to address these arguments in the Response to Arguments section.

Additionally, Murty fails to disclose that the interrupt-handling (or "assigned") processor is operable to initiate the release of every other processor (or non-interrupt handling processors) from the interrupt mode on a timed release basis **following** the **completion** by the interrupt-handling processor of the **processing tasks** associated with the interrupt. This element is taken from now-cancelled dependent claim 5. Murty, at best, teaches that the first of the logical processors to access a shared register handles the interrupt; the remaining logical

processors, detecting that the interrupt has been claimed by the first logical processor, return from the interrupt handler *on their own*; and the first logical processor *continues executing the interrupt-handler*. (Murty, [0049]) Thus, it is clear from Murty that the release of the non-interrupt handling processors is **not** initiated by the interrupt-handling processor **following** the **completion** by the interrupt handling processor of the processing tasks associated with the interrupt. The processor handling the interrupt in Murty *continues* executing the interrupt-handler *while* all the other processors exit the interrupt handler. (Murty, [0049])

Because Murty fails to disclose the claimed element of the non-interrupt handling processors being operable to be serially released from the interrupt mode according to a **timed release basis following** the **completion** by the interrupt-handling processor of the **processing tasks** associated with the interrupt, Murty fails to support a finding of anticipation under 35 U.S.C. 102(b). Applicant requests that this rejection be withdrawn. Claims 3, 4, and 6 depend directly or indirectly from independent claim 1 and are therefore allowable for at least the same reason.

B. Claims rejected under 35 U.S.C. 103

Claims 7-15, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles. Independent claims 7 and 17 each require, in part, that the interrupt-handling processor initiates the serial exit of the non-interrupt handling processors from the interrupt mode **following** the **completion** by the interrupt-handling processor of the **processing tasks** necessary to resolve the interrupt. As stated above with respect to independent claim 1, Murty fails to teach or suggest this element. The Examiner does not point to Giles to remedy this deficiency. Giles, at best, teaches that processors enter a debug mode as a result of

one processor asserting a single debug event signal. (Giles, Abstract). Giles does not teach or suggest all of the required elements of independent claims 7 and 17.

Thus, the combination of Murty and Giles fails to teach or suggest that the interrupt-handling processor initiates the serial exit of the non-interrupt handling processors from the interrupt mode **following** the **completion** by the interrupt-handling processor of the **processing tasks** necessary to resolve the interrupt. Because all of the elements of independent claims 7 and 17 are not taught or suggested by the combination of Murty and Giles, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Giles, all of the claimed limitations of independent claims 7 and 17 are not shown in the combination. Applicant respectfully submits that the rejection of claims 7 and 17 should be withdrawn and that these claims should be passed to issuance. Claims 8-16 and 18-20 depend directly or indirectly from independent claims 7 and 17 and are therefore requested to be passed to issuance for at least the same reasons.

Conclusion

Applicant respectfully submits that claims 1, 3, 4, 6-8, and 10-20 should be passed to issuance.

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